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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,509	08/07/2003	Masahiro Tada	241246US2	8468

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EXAMINER	
ABDULSELAM, ABBAS I	
ART UNIT	**PAPER NUMBER**
2629	

DATE MAILED: 10/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/635,509	TADA ET AL.	
	Examiner	Art Unit	
	Abbas I. Abdulselam	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 9-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4,20 and 21* is/are allowed.

6)☒ Claim(s) *9-15* is/are rejected.

7)☒ Claim(s) *16-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 2/16/05, 11/18/04, 8/7/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to a communication filed on 07/20/06. Claims 1-4 and 9-21 are elected in response to a restriction requirement, and the examination of those claims results in as follows.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 9-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawazoe et al. (USPN 6524893) in view of Toshiro et al (USPN 5021694).

Regarding claim 9, Kawazoe (USPN 6524893) teaches an optical sensor diode, (trigger diode as an electrostatic discharge protection device, Fig. 1, col. 10, lines 7-10) comprising: a semiconductor layer including a p region to which p-type impurities are injected, (P-type anode high impurity concentration (4), col. 10, lines 11-12) an n region to which n-type impurities are injected (an n-type anode gate high impurity concentration region (5), col. 10, lines 12-13) and; an anode electrode connected to the p region; (p-type anode, col. 10, line 12) a cathode electrode connected to the n region; (n-type cathode, col. 10, line 16) and a gate electrode provided above the i region with an insulating film interposed therebetween (polysilicon (14), gate side wall insulators (12) form a gate of MOS transistor, col. 10, lines 29-33).

Kawazoe does no teach an i region with a lower impurity concentration than those of the p and n regions.

Toshiro et al (USPN 5021694) on the other hand teaches means being provided between the p or n-gate electrode on a gate region, which is lower in its impurity density than the other gate region (see the abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kawazoe's electrostatic discharge protection device shown in Fig. 1 to adapt Toshiro's means of providing lower impurity density as illustrated in Fig. 3 because the use of low impurity density helps drive a circuit with a gated p-n-p-n device as taught by Toshiro (see the abstract).

Regarding claim 10, Kawazoe teaches the semiconductor layer is formed of polysilicon (col. 10, lines 29-33, fig. 1(14)).

Regarding claim 11, Kawazoe teaches the p-type impurities are boron and the n-type impurities are phosphorous (p-type semiconductor containing a low concentration of boron is used, n-type is described in terms of different impurity col. 10, lines 1-6. It would have been obvious to one of ordinary skill in the art to utilize kawazoe's teaching of different impurity for the purpose of selecting the type of impurity to be used)

Regarding claim 12, Toshiro teaches another n region, to which n-type impurities are injected at a lower concentration than that of the said n region, between the i region and the said n region (It would have been obvious to utilize Toshiro's lower impurity density).

Regarding claim 13, Kawazoe teaches the gate electrode is connected to the cathode electrode (a polysilicon to be a gate electrode of the MOS transistor, col. 5, lines 9-23).

Regarding claim 14, Kawazoe teaches the gate electrode is connected to the anode electrode (a polysilicon to be a gate electrode of the MOS transistor, col. 5, lines 9-23).

Regarding claim 15, Kawazoe teaches a first electrostatic capacity element formed between the gate electrode and the anode electrode; and a second electrostatic capacity element formed between the gate electrode and the cathode electrode (a first and a second electrostatic discharge protection circuits, col. 7, lines 1-20).

Allowable Subject Matter

4. Claims 16-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 1-4 and 20-21 are allowed.

Reasons for Allowance

6. Kawazoe et al. (USPN 6524893) teach a trigger diode wherein an n-type well 2 is provided in a p-type substrate 1. A p-type anode high impurity concentration region 4 and an n-

type anode gate high impurity concentration region 5 are provided on the surface of the n-type well 2. A p-type cathode gate high impurity concentration region 7 and an n-type cathode high impurity concentration region 6 are provided on a portion of the surface of the p-type substrate 1 which is away from the n-type well 2. A silicide layer 10 is provided on the surface of each of the p-type anode high impurity concentration region 4, the n-type anode gate high impurity concentration region 5, the p-type cathode gate high impurity concentration region 7, and the n-type cathode high impurity concentration region 6. The silicide layer 10 is connected to a metal 17, 18 or 19 via a contact 16 (See Fig. 1).

Regarding claim 1, prior art does not teach a display device, comprising: switching elements for driving pixels that are formed at the respective intersections of signal lines and scan lines; and photoelectric conversion elements that are provided at least one by one while corresponding to the switching elements respectively and which convert light received within a specified range into an electric signal, wherein the photoelectric conversion element has an I layer between a p layer and an n layer, and a defect density of this I layer is higher than a defect density of a channel portion of the switching element.

Regarding claim 20, prior art does not teach an image acquisition circuit, comprising: a plurality of signal lines installed on a glass insulating substrate; a plurality of selective lines installed so as to intersect with the signal lines; a common control line installed corresponding to each of the selective lines; selection switches provided for the respective signal lines; and gate-controlled type optical sensor diodes provided at the respective intersections of the signal lines and the selective lines, in which from an anode electrode and a cathode electrode, one is selected

to be connected to the signal line, and the other one is connected to the selective line, and a gate electrode is connected to the common control line.

Regarding claim 21, prior art does not teach a method for driving an image acquisition circuit which has a plurality of signal lines installed on a glass insulating substrate, a plurality of selective lines installed so as to intersect with the signal lines, a common control line installed corresponding to each of the selective lines, selection switches provided for the respective signal lines and gate-controlled type optical sensor diodes provided at the respective intersections of the signal lines and the selective lines, in which from an anode electrode and a cathode electrode, one is selected to be connected to the signal line, and the other one is connected to the selective line, and a gate electrode is connected to the common control line, the method comprising the steps of: applying a fixed voltage to the common control line; turning on a selection switch of a signal line to which an optical sensor diode for detecting the amount of light is connected; and applying a voltage larger than the fixed voltage to a selective line to which the optical sensor diode for detecting the amount of light is connected.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following arts are cited for further reference.

U.S. Pat No. 5,596,217 toYamaoka et al.

U.S. Pat. No. 5,202,573 to Shirai

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abbas I. Abdulselam whose telephone number is 571-272-7685. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Abbas Abdulselam

Examiner

Art Unit 2629

10/04/06

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600